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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/545,785	04/07/2000	Tirdad Sowlati	US 000099	2253

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/545,785	SOWLATI ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,9 and 11-21* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 13, 14 and 21 are objected to because of the following informalities: The term "screen" was not defined in the disclosure in such a way as to clarify the description of the plate structures. The examiner suggests to use the term "mesh". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

1. Claims 1-6, 8-9 and 11-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ng et al. (5,583,359).

Regarding claims 1-3, Ng et al. teach in figure 8 and related text a capacitor 200 over a substrate 202 comprising a first level 210 of at least four electrically conductive parallel lines extending in a first direction and lying in a first plane, the first plane disposed above a substrate,

at least a second level 212 comprising metal or polysilicon (column 9, lines 65-66) of at least four electrically conductive parallel lines extending in the first direction and lying in a second plane above the first plane, each of the second level lines being

disposed over a respective one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four coplanar line pairs, each line pair comprising one of the first level lines and a respective one of the second level lines, the coplanar line pairs being substantially parallel to, and extending vertically upward from the substrate;;

a dielectric layer 250 (figure 9) disposed between the first and second levels of conductive lines;

a plurality of vias 230 arranged in a plurality of groups, each group corresponding uniquely to one of the coplanar line pairs and each group including at least two vias connecting the first level line and the second level line of the corresponding line pair (6 vias per line are depicted in figure 8), thereby forming an array of at least vertically oriented parallel capacitor plates, the vertically oriented parallel screen plate structures being spaced apart from each other and only dielectric material being disposed between each of the vertically oriented parallel plates; and

electrically opposing nodes forming the terminals of the capacitor, the array of vertically oriented parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities (figures 10-11).

Figure 8 does not depict an array of at least four parallel capacitor plates. Figure 10 depicts a capacitor comprises plurality of parallel capacitor plates (fingers) of alternating polarity. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an array of at least four parallel capacitor plates in Ng et

al.'s device, in order to adjust the capacitance of the device according to the requirements of the application in hand.

Regarding claim 4, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a dielectric layer comprising silicon dioxide in Ng et al.'s device, because silicon dioxide is a conventional dielectric material, of which judicial notice may be taken.

Regarding claims 5, 6, 14 and 19, Ng et al. teach in figure 8 at least a third level 214 of at least four electrically conductive parallel lines extending in the first direction and lying in a third plane above the first and second planes such that each of the third level lines is coplanar with a respective one of the line pairs, and a second dielectric layer 252 (figure 9) disposed between the second and third levels of conductive lines so that the third level of lines vertically extends the array of at least four parallel capacitor plates.

Regarding claims 8-9 and 11, Ng et al. teach a capacitor being formed using known CMOS techniques (column 2, lines 56-57). Therefore, the capacitor comprises a sub-micron CMOS structure, as claimed.

Regarding claims 12 and 15, Ng et al. teach in figure 8 a plurality of vias 230 arranged opposite a next respective plurality of vias, with identical spacing of vias in each plurality of vias.

Regarding claims 13 and 18, Ng et al. teach in figure 8 a plurality of vias 230 directly connecting the first level line and the second level line of corresponding line pair.

Regarding claims 16 and 20, Ng et al. teach in figure 8 each group includes four vias.

Regarding claim 17, Ng et al. teach in figure 8 first and second vias connecting the first level line and the second level line of corresponding line pair at respective first and second ends of the first and second level lines, respectively, wherein the second ends are opposite the first ends along the first direction.

Allowable Subject Matter

Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for allowance

The following is an examiner's statement of reasons for allowance: Ng et al. appear to be the closest prior art reference. Ng et al. teach substantially the entire claimed structure, as recited in claim 1, except a capacitor plate structure comprising a mesh

structure. Therefore, prior art do not teach or render obviousness the semiconductor structure, as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments with respect to claims 1-9 and 11-21 have been considered but are moot in view of the allowance claims which include the limitation of a capacitor plate structure comprising a mesh structure.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
March 16, 2004

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800